

1 1. (Amended) A memory module controller for [interfacing a plurality of
2 memory device on a memory module with a system memory bus coupled to a
3 system memory module, the memory module controller] providing an interface
4 between a system memory controller and a plurality of memory devices on a
5 memory module, comprising:
6 first interface circuitry configured to receive from the system memory
7 [bus] controller a first memory transaction [having] in a first format; and
8 control logic coupled to the first interface circuitry and configured to convert
9 the first memory transaction into [generating] a second memory transaction in a
10 second format for the plurality of memory devices, wherein the second format of
11 the second memory transaction [corresponds to the first memory transaction and
12 has a second format] is different [than] from the first format of the first memory
13 transaction.

1 2. (Amended) The memory module controller of claim 1, further comprising:
2 second interface circuitry coupled to the control logic and configured to
3 transmit the second memory transaction to at least one of the plurality of memory
4 devices.

1 3. (Amended) The memory module controller of claim 1, wherein the first
2 memory transaction includes time multiplexed address and command information.

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1 4. (Amended) The memory module controller of claim 3, wherein the first
2 interface circuitry comprises:
3 request handling logic [that separates] configured to separate the address
4 and command information and [provides] to provide the separate address and
5 command information to the control logic.

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1 5. (Amended) The memory module controller of claim 4, wherein the first
2 memory transaction further includes time multiplexed data information, and
3 wherein the request handling logic is further configured to separate the time
4 multiplexed data information and [provides] to provide the [separate] separated
5 time multiplexed data information to the control logic.

1 6. (Amended) The memory module controller of claim 1, wherein the first
2 interface circuitry comprises:
3 handshaking logic configured to provide [provides] a handshake signal to
4 the system memory [bus] controller that indicates when the memory module
5 controller is communicating data to the system memory [bus] controller.

1 7. (Amended) The memory module controller of claim 1, wherein the first
2 interface circuitry comprises:
3 data handling logic configured to receive data [of] for the first memory
4 transaction from the system memory [bus] controller and reformat the data for the
5 second memory transaction.

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1 8. (Amended) The memory module controller of claim 1, further comprising:
2 a write buffer coupled to the first interface circuitry and configured to store
3 [storing] data sent with the first memory transaction.

1 9. (Amended) The memory module controller of claim 8, further comprising:
2 an address storage unit coupled to the write buffer and the first interface
3 circuitry[,] and the address storage unit is configured to store [storing] addresses
4 associated with the [write] data stored in the write buffer.

1 10. (Amended) The memory module controller of claim 1, further comprising:
2 a read buffer coupled to the control logic[, the read buffer] and configured to
3 store [storing] data read from at least one of the plurality of memory devices.

1 11. (Amended) The memory module controller of claim 1, further comprising:
2 a clock generator circuit coupled to the control logic and configured to
3 receive a first clock signal from the system memory [bus] controller[, the clock
4 generator circuit generating] and to generate a second clock signal for the plurality
5 of memory devices.

1 12. (Amended) A memory module controller for [interfacing a plurality of
2 memory device on a memory module with a system memory bus coupled to a

3 system memory module, the memory module controller] providing an interface
4 between a system memory controller and a plurality of memory devices on a
5 memory module, comprising:
6 means for receiving from the system memory [bus] controller a first
7 memory transaction [having] in a first format; and
8 means for [generating] converting the first transaction into a second memory
9 transaction in a second format for the plurality of memory devices, wherein the
10 second format of the second memory transaction [corresponds to the first memory
11 transaction and has a second format] is different [than] from the first format of the
12 first memory transaction.

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1 13. (Amended) A memory module controller for [interfacing a plurality of
2 memory devices on a memory module with a system memory bus coupled to a
3 system memory module, the memory module controller] for providing an
4 interface between a system memory controller and a plurality of memory
5 devices on a memory module comprising:
6 first interface circuitry configured to receive from the system memory
7 [bus] controller a first memory transaction in a first format; and
8 control logic coupled to the first interface circuitry and configured to reformat
9 [reformatting] the first memory transaction [transactions] such that [for] the plurality
10 of memory devices perform the reformatted first memory transaction.